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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,623	09/30/2003	William B. Schwartz	RPS92030116US1	6348

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EXAMINER	
WEINMAN, SEAN M	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,623	SCHWARTZ ET AL.	
	Examiner	Art Unit	
	Sean Weinman	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. ***Claims 1-16*** are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. ***Claim 1*** is rejected under 35 U.S.C. 102(b) as being anticipated by Takashima et al. (US Patent No. 6,347,372).

4. ***As per claim 1***, Takashima et al. teach the claimed invention, comprising:

A system capable of dynamically configuring a multi-node computer *(Figure 4)*, the system comprising:

a plurality of processor nodes *(Figure 4 Reference characters 31, 311,312, and 313)*; and

a scalability management module directly coupled to each of the plurality of processor nodes *(Figure 4 Reference characters 42 and 45)*, the scalability management module including:

a dedicated processor for managing the plurality of nodes, the dedicated processor not being from the plurality of processor nodes *(Figure 4 Reference character 35 and Col. 7 lines 26-39 Takashima et al does not explicitly detail a dedicated processor but it is inherent that a dedicated processor must exist within the processor status detection unit for the processor status detection unit to detect the processor*

status, processor description, boot request application type, boot length, boot speed, boot completion, and block transmission result) ; and

a scalability chipset for enabling the dedicated processor to dynamically configures the plurality of nodes into a coordinated multi-node computer *(Figure 4 Reference character 45 Col. 6 line 52-67 and Col. 7 line 1-39)*,

wherein the multi-node computer is configured by the scalability management module without a re-wiring of connections between processor nodes during a subsequent reconfiguration of the multi-node computer *(Figure 4 Reference character 30 Col. 7 lines 3-20 The boot data loaded to configure the specific processor is sent over the shared bus from the memory)*.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. ***Claims 5, 9, and 13*** rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Takashima et al. (US Patent No. 6,347,372) in view of Dove et al. (US Patent No. 5,938,765).

7. ***As per claim 5***, Takashima et al. teach the claimed invention for all of the reasons stated above. Takashima et al., however, does not teach performing a full boot on a host processor node. In summary, Takashima et al. teaches a plurality of processor nodes that are coupled to a scalability module comprising a dedicated

processor to configure the plurality of processor nodes and perform a primary boot on the plurality of processor nodes. Takashima does not teach a host processor node to complete a full boot of the system.

8. Dove et al. teach a method for booting up a multi node multiprocessor computer system where a single processor from the any of the processor nodes in the system is a host processor to complete a full boot of the complete system. Dove et al. teach the claimed invention comprising:

completing a full boot on a host processor node, the host processor node being selected by the scalability management module from the plurality of processor nodes, to enable the host processor node to control the multi-node computer *(Col. 7 lines 4-22)*. In summary, Dove et al. teaches a method of completing a full boot to a multi node multiprocessor computer system on a master processor from one of the plurality of processor nodes.

9. It would have been obvious to combine the teachings of Takashima et al. and Dove et al. because they both teach methods of booting multi node multiprocessor computer system. Dove et al. teaches the deficiency of Takashima et al. by teaching a host processor node completes a full boot of the computer system.

10. ***As per claim 9***, it is directed to the computer program product of the method for dynamically configuring a multi node computer system as set forth in claim 5. Since Takashima et al. and Dove et al. teach the claimed method of reconfiguring a multi node computer system, Takashima et al. and Dove et al. teach the computer program product for configuring a multi node computer system.

11. ***As per claim 13***, it is directed to the service for the method for dynamically configuring a multi node computer system as set forth in claim 5. Since Takashima et al. and Dove et al. teach the claimed method of reconfiguring a multi node computer system, Takashima et al. and Dove et al. teach the service for configuring a multi node computer system.

12. ***As per claim 2, 6, 10, and 14***, Takashima et al. and Dove et al. teach the claimed invention, comprising:

13. Takashima et al. teach the claimed invention, comprising:

the scalability chipset *(Figure 4 Reference character 45)* comprises: a memory controller and a scalability controller (*Figure 4 Reference character 33 and 35 Takashima et al. does explicitly detail a memory controller but it is obvious that a memory controller must exist to control the accessing of the boot data within the memory)*

14. Dove et al. teach the claimed invention, comprising:

a host bridge controller within the scalability chipset *(Col. 11 lines 9-11 Dove et al. does not explicitly detail the host bridge controller within the scalability chipset Lee et al. does teach the configuration controls on each node having a host bridge controller. It would have been obvious to one of ordinary skill in the art to have a host bridge controller within the scalability chipset rather than each processor node).*

15. ***Claims 3, 7, 11, and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima et al. (US Patent No. 6,347,372) in view of Dove et al.

(US Patent No. 5,938,765) as applied to claims 5, 9, and 13 above, and further in view of Stallmo et al. (US Patent No. 5,689,678).

16. ***As per claims 3, 7, 11, and 15***, Takashima et al. and Dove et al. teach the claimed invention for all of the reasons stated above. Takashima et al. and Dove et al., however, does not each teach that a spare hot node can be configured if the processor node fails or is removed from the system. In summary, Takashima et al. and Dove et al. teach a plurality of processor nodes that are coupled to a scalability module comprising a dedicated processor to configure the plurality of processor nodes and perform a primary boot on the plurality of processor nodes. Takashima et al. and Dove et al. does not teach the system having a hot spare node to be configured if a processor node fails or is removed.

17. Stallmo et al. teaches multiprocessor computer system having multi modules, each module with a individual processor, and additionally having a spare node to be configured if the processor node were to fail. Stallmo et al. teach the claimed invention comprising:

the plurality of processor nodes includes a hot spare node capable of being configured by the scalability management module if another of the processor nodes fails or is removed from the multi-node computer *(Figure 2 and Col. 8 lines 46-51 and Col. 18 lines 59-76 and Col. 19 lines 1-9 The MCU has its own individual processor)*. In summary, Stallmo et al. teach a system having a hot spare node to be configured if a processor node fails or is removed.

18. It would have been obvious to one of ordinary skill in the art to combine the teachings of Takashima et al. and Dove et al. and Stallmo et al. because they all teach multi node multiprocessor computer system with the ability to configure each node individually. Stallmo et al. teaches the deficiency of Takashima et al. and Dove et al. by teaching a hot spare node capable of being configured if another of the processor nodes fails or is removed.

19. ***Claims 4, 8, 12, and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima et al. (US Patent No. 6,347,372) in view of Dove et al. (US Patent No. 5,938,765) as applied to claims 5, 9, and 13 above, and further in view of Golden et al. (US Patent No. 6,681,282).

20. ***As per claims 4, 8, 12, and 16***, Takashima et al. and Dove et al. teach the claimed invention for all of the reasons stated above. Takashima et al. and Dove et al., however, does not each teach a remote logic which is able to control the configuration of the multi node computer through the scalability management module. In summary, Takashima et al. and Dove et al. teach a plurality of processor nodes that are coupled to a scalability module comprising a dedicated processor to configure the plurality of processor nodes and perform a primary boot on the plurality of processor nodes. Takashima et al. and Dove et al. do not teach the system having remote manager logic to control the configuration of the multi node computer.

21. Golden et al. teach a multiprocessor computer system having remote manager logic to control the configuration of the multiprocessor nodes. Golden et al. teach the claimed invention comprising:

a remote manager logic coupled to the scalability management module, wherein the remote manager logic controls the configuration of the multi-node computer via the scalability management module *(Figure 8 Col. 9 lines 18-67 and Col. 10 lines 1-35 The server management console (SMC) controls all the functions of the server management platform (SMP Figure 8 Reference character 800) including the microprocessor system manager (MBM) which controls the function of the individual processor nodes. The SMC is connected to the MBM through a LAN Ethernet line)* In summary, Golden et al. teaches a system having remote manager logic to control the configuration of the multi node computer.

22. It would have been obvious to one of ordinary skill in the art to combine the teachings of Takashima et al. and Dove et al. and Golden et al. because they all teach multi node multiprocessor computer system with the ability to configure each node individually. Golden et al. teaches the deficiency of Takashima et al. and Dove et al. by teaching a multiprocessor computer system having remote manager logic to control the configuration of the multiprocessor nodes.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115

CHUN CAO
PRIMARY EXAMINER